Wait State Processing on the Heathkit HA-8-3 Color Graphics Card

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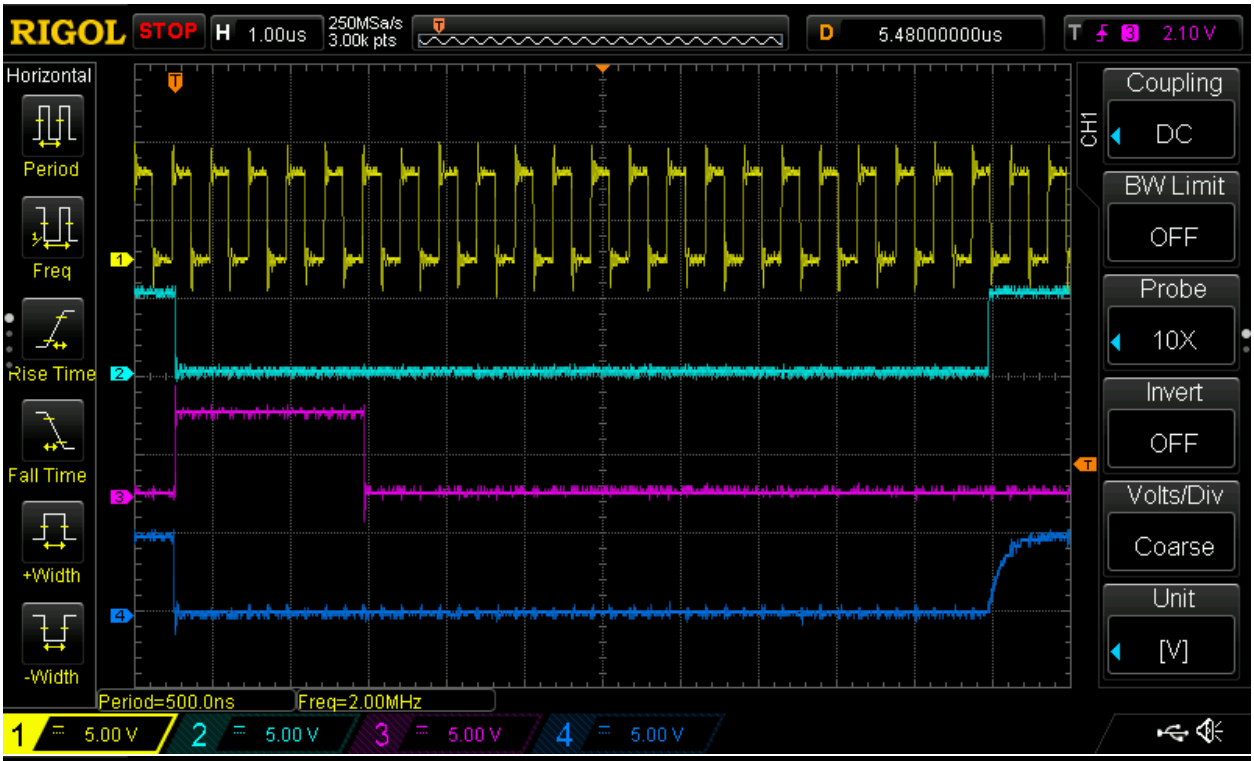
March 29, 2022

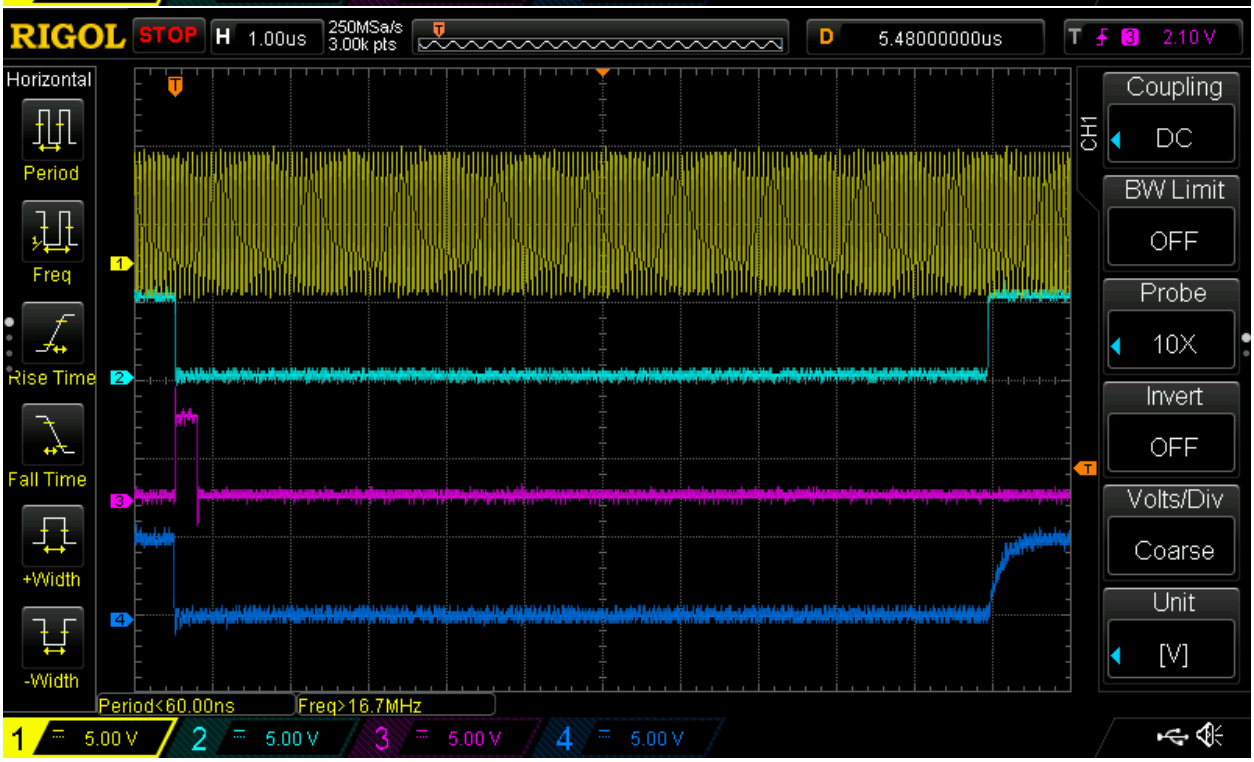
ADC Wait States

Yellow: Bus Clock, Cyan: AD_BUSY, Magenta: AD_WAIT, Blue: RDYIN*

TOP: 2MHz CPU speed, BOTTOM: 16MHz CPU speed

NOTE: The AD7574 BUSY signal causes the CPU to enter a wait state until the conversion is complete – this period is not affected by the CPU speed. The purpose of the AD_WAIT signal was to guarantee the CPU entered the WAIT state while waiting for the AD7574 to assert its BUSY signal. The length of AD_WAIT is CPU speed dependent.



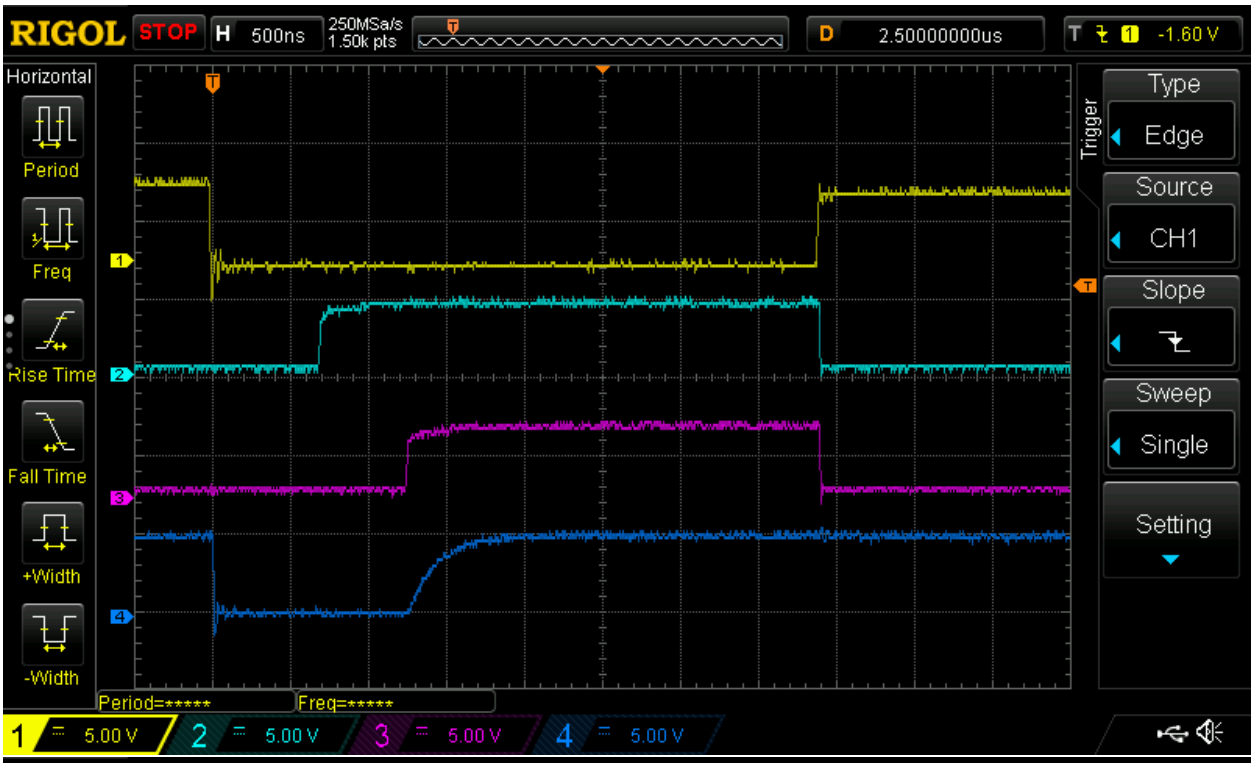


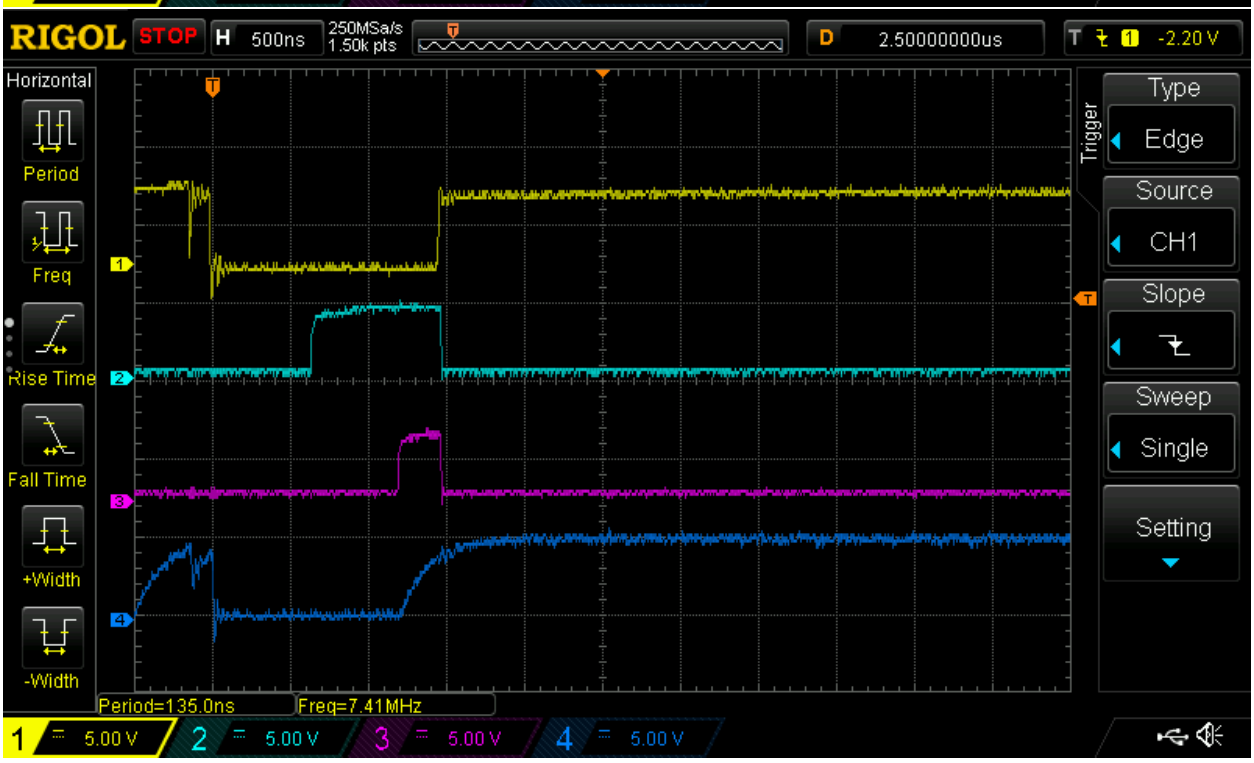
PSG Wait States

Yellow: PSGSEL, Cyan: PSG ENABLE, Magenta: PSG DONE, Blue: RDYIN*

TOP: 2MHz CPU speed, BOTTOM: 16MHz CPU speed

NOTE: Shift register U37 counts “Colorburst Clock” (JP15) cycles starting with the PSGSEL pulse. Three clock cycles after PSGSEL, PSG ENABLE goes active, two cycles after that PSG DONE goes active. The CPU is held in wait state until PSG DONE. The trailing edge of PSGSEL resets the ENABLE and DONE signals. The length of the wait state is independent of the CPU clock (compare the BLUE trace between the two images). The PSG has two clock cycles between ENABLE and DONE to access the bus.



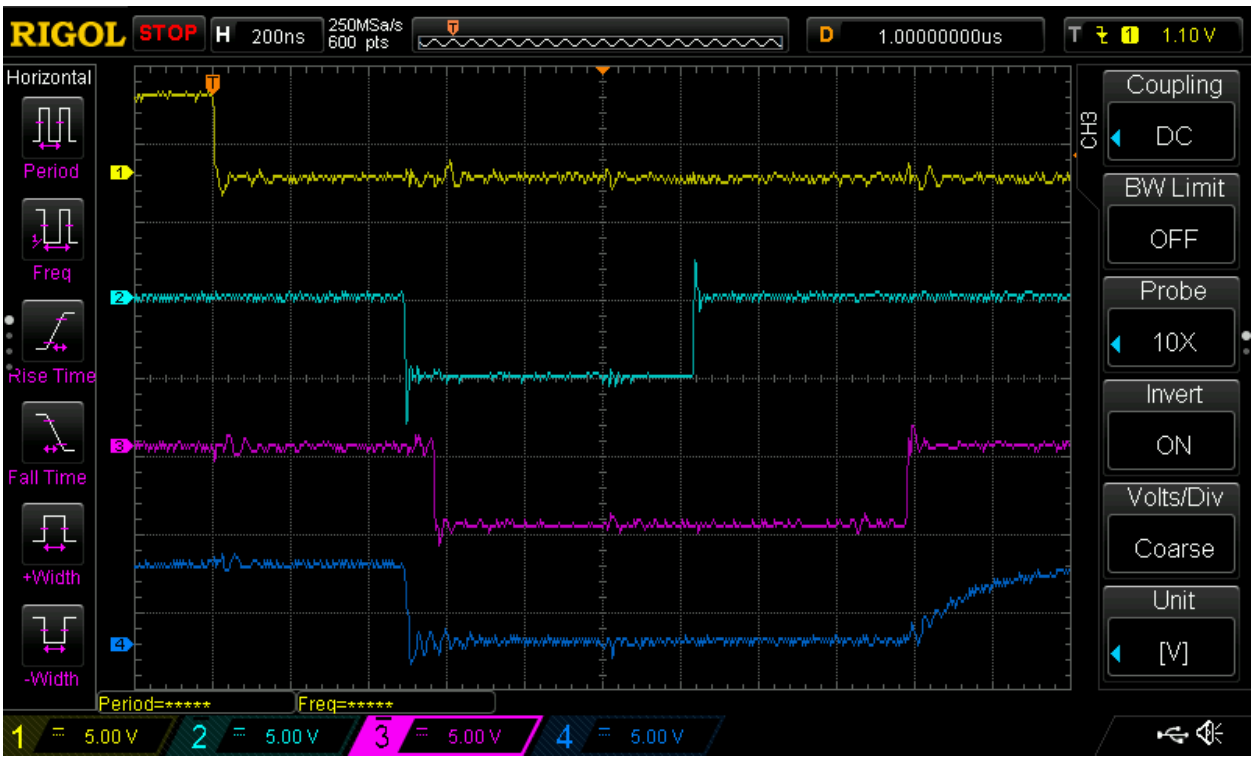


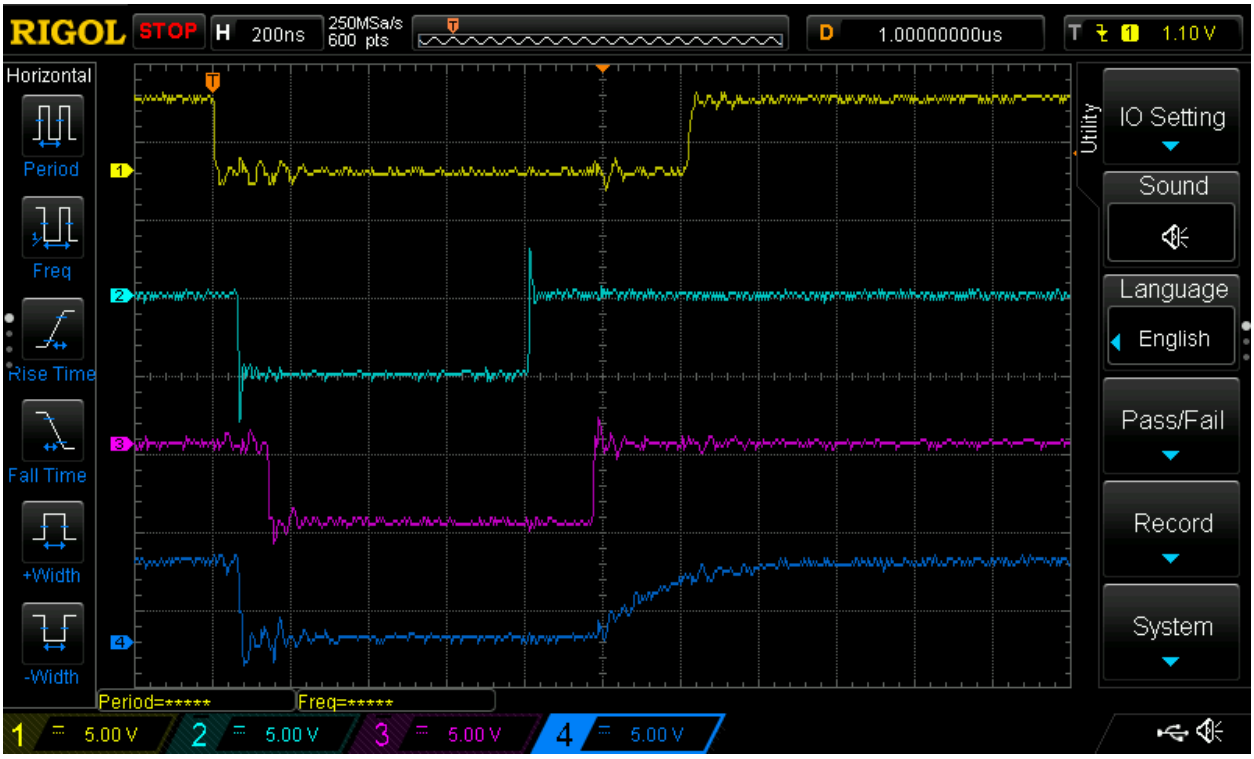
APU Wait States

Yellow: APUSEL, Cyan: I/O WAIT, Magenta: APU_WAIT, Blue: RDYIN*

TOP: 2MHz CPU speed, BOTTOM: 16MHz CPU speed

NOTE: The general I/O WAIT (from the onboard wait state generator, or the comparable System Support I generator) holds the CPU until the APU can assert its PAUSE (APU_WAIT) signal. The length of the PAUSE depends upon the APU instruction being executed. None of this depends upon the CPU clock speed.





These APU traces also show the difference between generating Chip Select based only on address lines (APUSEL, yellow line) compared to ANDing the address selection with IORQ (the leading edge of the general I/O Wait pulse, Cyan line, aligns with the leading edge of the IORQ pulse). The chip select can be generated one full clock cycle ahead of the IORQ pulse. This is required to meet the AM9511 timing specification, and it was also found to be necessary for some older, slower 8255s to work on the PPIO card.

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March 29, 2022